

Derek Le

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EDUCATION

BS Computer Engineering with Honors, Digital Hardware Concentration — UC Santa Cruz

Minor in Electrical Engineering | GPA: 3.37 | Graduated June 2026

Relevant Coursework: Intro to VLSI, ASIC Systems Design, Computer Architecture, Logic Design

PROJECTS

Approximate Softmax Accelerator — Individual ASIC Design (Tiny Tapeout Sky130 template)

- Designed RTL in Verilog for a small accelerator that runs softmax, a core neural-network math step, using a finite-state machine to step through each stage.
- Verified the design in simulation with self-checking cocotb testbenches in Python on Icarus Verilog, checking 27 test cases against a reference model.
- Synthesized the design with Yosys and replaced a planned reciprocal circuit with a small lookup table, giving up a little accuracy to fit Tiny Tapeout's size limit.

FPGA Video Game — Course Project, UCSC (SystemVerilog / Basys-3)

- Built an FPGA video game in SystemVerilog, designing all of its digital logic from scratch: a state machine for game rounds, VGA video output, and moving sprites that collide.
- Verified timing with static timing analysis in Vivado, confirming the design met its 100MHz clock so it would run reliably on the board.

ASIC Systems Design — Course Labs, UCSC (CSE 225)

- Designed clock-domain-crossing (CDC) FIFO RTL in SystemVerilog that passed audio safely between two parts of a chip running at different clock speeds.
- Debugged planted bugs in basic logic blocks by writing black-box testbenches and tracing failures in Icarus Verilog and Verilator simulation.
- Integrated open-source UART, AXI-Stream and AXI IP into two small FPGA systems-on-chip, then wrote cocotb tests confirming data moved correctly both ways.

WORK EXPERIENCE

VnResource — Software Engineering Intern, Saigon, Vietnam (July–Aug 2024)

- Built an educational chatbot with a Python backend alongside a cross-functional software team, giving instructor-specific answers for schools in Vietnam.

SKILLS

Languages: Verilog, SystemVerilog, Python, C

EDA & simulation: Vivado, Yosys, cocotb, Icarus Verilog, Verilator

Protocols, lab & tools: I2C, UART, AXI-Stream, oscilloscope, soldering, Linux, Git